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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/839,013	04/21/2001	Leon Lee Chen	ADTST.021AUS	1329

7590 02/20/2004

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EXAMINER	
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ART UNIT	PAPER NUMBER
2133	4

DATE MAILED: 02/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/839,013	Applicant(s) CHEN ET AL.	
	Examiner Mujtaba K Chaudry	Art Unit 2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 April 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 April 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings are objected to because:

- Figures 1A-1D should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.
- Figures 2A-2D should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 3 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim language states in part, "...a software configured to respond to the interrupt

signal through the host computer **in a timely fashion with a minimal time latency and with high priority**." Theses are not positive limitations and therefore Applicant is advised to amend or cancel the present claim.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rhodes (USPN 5557559).

As per claims 1 and 8, Rhodes substantially teaches (title and abstract) a burn-in system for the accelerated life testing of semiconductor devices, of the type including a burn-in driver universally reconfigurable by computer control, a computer software system and method combining interactive systems for designing projects having data for reconfiguring the driver, designing test sequences having data for controlling semiconductor burn-in, designing oven chamber and driver and burn-in board configurations for use in burn-in control, controlling burn-in testing, diagnosing hardware problems, and providing system security. The software system of a multi-purpose computer controlled driver system functions with and controls the

burn-in system hardware to accomplish the signal conditioning and testing during the same time period of a wide variety of devices quickly and efficiently with a minimum of system setups. Rhodes teaches (Figure 2) a simplified block diagram of a computer-controlled burn-in system which incorporates a universal driver system and which is controlled by operating software. In Figure 2, an external computer 50 (analogous to host computer of the present application) is coupled to a plurality of universal driver systems 100 (analogous to device driver of the present application) via computer bus 52. Each of the universal driver systems 100 is coupled to a burn-in board 500 by a plurality of input and output signal paths which provide the required digital and analog signals to properly control, exercise and monitor the devices under test (DUT's) that are mounted on each burn-in board. Output signal paths which couple from each of the universal driver systems 100 to a burn-in board 500 include power bus 115, analog bus 120 and vector/monitor bus 125. Input signal paths which couple from each burn-in board 500 to a universal driver system 100 include DUT monitors bus 127 and automatic programming bus 129. Each burn-in board 500 also includes an identification code means 501, which couples to the associated driver system 100 via automatic programming bus 129. Identification code means 501 allows each burn-in board 500 to be uniquely identified by the operating software, which is resident and functioning in external computer 50 so that particular sets of stored instructions, and data can be- loaded into a particular driver system 100. These sets of stored instructions and data cause the reconfiguring of the electrical properties of the driver system 100 appropriate for the particular devices under test that are installed in the particular burn-in board 500 which is coupled to the driver system 100. Thus the electrical properties of the driver system 100 can be changed by the control exercised by the operating system software of the

present invention to meet the requirements of the particular devices under test that are installed in the particular burn in board 500 which is coupled to the driver system 100 without any hardware change or reconfiguration. Furthermore, Rhodes teaches (Figure 3) a block diagram of the universal driver system 100 and the primary controllable hardware device which is controlled by the computer system. In FIG. 3, a computer bus 52 (a bi-directional bus) couples from an external computer 50 (see FIG. 2) to computer interface module 101. Computer interface module 101 contains address logic circuitry which determines that driver data present on computer bus 52 is received by the correct one of a plurality of the universal driver system 100. Computer interface module 101 also contains the transceiver and select logic circuitry required to provide direction and control for data being transferred from external computer 50 to the particular modules which comprise universal driver system 100 and, conversely, for data being transferred from the particular modules which comprise universal driver system 100 to external computer 50. Computer interface module 101 is coupled to all of the plurality of other modules which make up universal driver system 100 by system bus 102 (a bi-directional bus). System bus 102 comprises a plurality of signal paths for transmitting and receiving the data and control signals required to control and reconfigures the other modules which make up universal driver system 100 of the present invention. Thus system bus 102 couples to power management module 103, system timing generation module 104, vector hold module 105, analog generation module 106, vector storage module 107, tri-state control module 108, automatic programming module 109, DUT monitoring module 110, and on-board status monitoring module 111.

Rhodes does not explicitly teach a hardware timer for producing an interrupt signal and the device driver to cause to start the test pattern upon receiving the interrupt signal as stated in the present application.

However, Rhodes teaches (col. 10, lines 27-66—col. 11, lines 1-32) that Burn-in stresses and vectors are test patterns and electrical signals that are provided to the DUT via the burn-in driver. Burn-in programs comprise profile of time, temperature and stress change provided during burn-in. Rhodes teaches (col. 4, lines 7-24) that a burn-in driver is an electronic device that provides the input, or stimulus, and monitors the output, to the DUT. A burn-in board (BIB) is a piece of hardware that provides both mechanical and electrical means of placing semiconductors in a burn-in chamber. A burn-in chamber is a physical enclosure that creates the burn-in environment. The chamber contains both the driver and BIB and may provide a harsh environment for the DUT. The burn-in driver generates complex electrical signals, called vectors. Vectors are then placed in a group called a pattern. In a typical burn-in system, the patterns provide signals that toggle the internal circuitry of the DUT, which exercise the internal transistors of the DUT. The *burn-in cycle is a combination of generated vectors, a temperature profile and the allotted time period.* There are two important file types unique to the system. First, a project file is a complete collection of configuration and vector pattern information that is later downloaded to the driver 100. Two components comprise the project: a Pattern, a collection of signals and vectors at a given address channel; and Latched Settings or Static parameters, i.e., voltage and frequency, that are set only once for a particular driver. Second, a sequence file is a group of Events and Actions that duplicate or extend the burn-in driver board's capability by allowing quick re-configuration of the driver 100. *The sequence allows the user to*

change DUT stresses based on time, temperature, or number of times that the test is run. Furthermore, Rhodes teaches (col. 20, lines 4-41) the goal of the sequence editor application 202 is to allow the user to create a sequence that exercises various features--i.e., voltage, frequency, etc.--of a particular driver type. The sequence editor 202 interacts with two other system software applications, the system controller 204 and the waveform editor 201. The sequence editor 202 takes the .prj file from the waveform editor 201 and places the information as an Action of a sequence. In this manner, the sequence editor application 202 creates a .seq file directly associated with the driver 100 tested by the system controller 204. *The sequence editor 202 creates a sequence of events that tests the DUT under specific parameters over a given period of time.* This application 202 allows for DUT testing in various controlled environments in one burn-in cycle. A sequence could be as simple as downloading a project or as complicated as setting voltages, frequencies, idle settings, vector delays and loops to repeat the test. The sequencing concept is a very powerful idea. Sequencing can accomplish almost all processes relating to the driver system. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a hardware timer for producing an interrupt signal and the device driver to cause to start the test pattern upon receiving the interrupt signal as stated in the present application. This modification would have been obvious to one of ordinary skill because one of ordinary skill would have recognized that a timing device would have been necessary in order to start and stop the test routines.

As per claims 2-4, 7, 9 and 12, Rhodes substantially teaches, in view of above rejections, (col. 20, lines 4-41) a sequence allows the user to change DUT stresses based on time, temperature, or number of times that the test is run. Furthermore, Rhodes teaches the goal of the

sequence editor application 202 is to allow the user to create a sequence that exercises various features--i.e., voltage, frequency, etc.--of a particular driver type. The sequence editor 202 interacts with two other system software applications, the system controller 204 and the waveform editor 201. The sequence editor 202 takes the .prj file from the waveform editor 201 and places the information as an Action of a sequence. In this manner, the sequence editor application 202 creates a .seq file directly associated with the driver 100 tested by the system controller 204. *The sequence editor 202 creates a sequence of events that tests the DUT under specific parameters over a given period of time.* This application 202 allows for DUT testing in various controlled environments in one burn-in cycle. A sequence could be as simple as downloading a project or as complicated as setting voltages, frequencies, idle settings, vector delays and loops to repeat the test. The sequencing concept is a very powerful idea. Sequencing can accomplish almost all processes relating to the driver system.

As per claims 5 and 10, Rhodes substantially teaches, in view of above rejections, (col. 17, lines 18-65) a waveform editor application 201 supports a vast array of editing features for creating or modifying bit wise signals. The user can modify or program vectors to meet a specific need. Functions include ANDing, COMPLEMENTing, INVERTing, ORing, XORing, pulse generation, and address generation. The waveform editor 201 maintains project control (see FIG. 10) by requiring the user of the project information screen 232 to enter version number (at 233), the day the project was created or revised (at 234), the person who did the editing (at 235), and comments (at 236). The user can modify many features of the waveform. Some of these features may include: latched based features (e.g., frequency, voltage, idle settings), flat vectors, hold channels, sub vectors, tri-state control, and scan control. The user has the ability to

create a digital channel, download the channels to a driver, and output the channels to a DUT as the drivers are run. The waveform editor 201 contains hold channels and flat vectors that are very simple to create and edit. In the system of the present invention, the user does not need extensive knowledge of the waveform editor 201 to modify or create a waveform. The modifications can be as simple as typing in a frequency or voltage change into the appropriate dialog box. The waveform editor display 208 graphically presents vector data in a timing diagram display. Various data points are displayed in waveform fashion with a different color for each information channel (see FIG. 11). The creation or editing of waveforms is just as easy. The user just has to click on a bit in the flat vector screen 235 and the vector is quickly changed (see FIG. 12). The user can choose which number base to enter the information about a particular waveform from the list dialog box located in the upper right hand corner of the screen (see FIG. 13): hexadecimal, decimal, binary, or octal. The user can also view the data in an addressed or time based format. In the preferred waveform editor 201 the user can input test data using Intel@ HEX, ASCII and Motorola@ S-record format, directly from the simulators and testers. The data is inputted automatically and mapped directly to the system hardware. Channel swapping supports simple and efficient re-mapping of signal output channels to the BIB. When selecting the tri-state mode in real-time, the signals graphically depict the tri-state levels. This feature determines when groups of signals are in the tri-state mode without reference to signal mapping charts.

As per claims 6 and 11, Rhodes substantially teaches, in view of above rejections, (col. 23, lines 12-60) the user can monitor more than one DUT during the burn-in cycle. During test, the system controller 204 records information (i.e. errors, if the driver is initiated, how many

DUTs are tested etc.) into a System Log File. The system reduces the steps of DUT monitoring. First, the user downloads the project to the driver 100. The driver 100 contains the test parameter information and the expected results of the test. The driver 100 is set in run mode. The driver 100 then sends the data to the DUT. Next, the information is received from the DUT. And last, *the driver 100 compares the expected results with the results from the test.* If the resultant information does not match the expected results the driver 100 records the mismatch as an error, otherwise the DUT passes.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Rhodes generally teaches testing of electronic components and more specifically to an improved system and method for the accelerated life testing of semiconductor devices in which the software system of a multi-purpose computer controlled driver system can function with and control the system hardware to accomplish the signal conditioning and testing of a wide variety of devices quickly and efficiently with a minimum of system setups and change-overs. Applicants are invited to read/review additional pertinent prior art that is included with this office action.

Any inquiries concerning this communication should be directed to the examiner, Mujtaba Chaudry who may be reached at 703-305-7755. The examiner may normally be reached Mon – Thur 7:30 am to 4:30 pm and every other Fri 8:00 am to 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, Albert DeCady at 703-305-9595. The fax phone number for the organization where this application is assigned is 703-746-7239.

Any inquiry of general nature or relating to the status of this application or proceeding should be directed to the receptionist at 703-305-3900.

Mujtaba Chaudry
Art Unit 2133
February 17, 2004

Guy J. Lamarre
for
Albert DeCady
Primary Examiner